



## ENDURING VALUE

PTO/SB/08A (10-01)

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Sheet	1	of	2
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**Complete if Known**

Application / Conf. No.	10/618,316	/	4779
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<b>Filing Date</b>	July 11, 2003
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First Named Inventor	Patrick Lysaght
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Art Unit	2825
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Examiner Name	Vuthe Siek
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Attorney Docket Number	X-1410 US
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## U.S. PATENT DOCUMENTS

[illegible]

**FOREIGN PATENT DOCUMENTS**

[illegible]

**Examiner  
Signature**

UNTHERSIEK

Date Considered

3/20/06

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Substitute for form 1449A/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				Application / Conf. No.	10/618,316 / 4779
				Filing Date	July 11, 2003
				First Named Inventor	Patrick Lysaght
				Art Unit	2825
				Examiner Name	Vuthe Siek
Sheet	2	of	2	Attorney Docket Number	X-1410 US

OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
VS		Monica Alderighi et al.; "A Fault-Tolerant FPGA-Based Multi-Stage Interconnection Network for Space Applications"; published Computer Society; pp. 1-5.	
VS		Ian Kyles; "Creating Large Switch Fabrics using the Three-Stage (Clos) Architecture"; Copyright VITESSE Semiconductor Corporation; pp. 1-12.	
VS		Steve Young et al.; "A High I/O Reconfigurable Crossbar Switch"; pp. 1-8.	

Examiner Signature	VUTHE SIEK	Date Considered	3/11/07
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